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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,877	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9 and 12* .
4) ■ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed December 2, 2002.

Response to Arguments

2. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because: a) in the body of the declaration it states "I hereby claim foreign priority..., by checking the box,...is claimed." Then above the box there is the heading "Priority Not Claimed." Please correct the inconsistencies.

Specification

4. The title of the invention is not **descriptive**. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a part of the insulating layer" (See Claims 1, 2, 10 and 11); b) "a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a laminate of the first insulating layer and the silicon oxide film" (See Claims 3 and 12); c) "first wiring line through an insulating layer" (See Claims 1 and 10); and d) "first wiring line through a first insulating layer" (See Claims 2, 3, 11 and 12). Claims 4-9 and 13-18 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-6 and 9 are rejected under 35 U.S.C. 103(a) as obvious over Hirabayashi et al. (U.S. Publication No. 2002/0093019) in view of Hashimoto et al. (U.S. Publication No. 2003/0038303).

In regards to claim 1, Hirabayashi et al. ("Hirabayashi") discloses the following:

a) the pixel TFF has a channel formation region (1a) formed above a first wiring line (11a) through an insulating layer, and has a low concentration impurity region (1b and 1c) that is in contact with the channel formation region and overlaps the first wiring line (For Example: See Figure 3); and

b) the storage capacitor (70) is formed from a capacitor wiring line (3b) formed on the same layer as the first wiring line (For Example: See Figure 3).

In regards to claim 1, Hirabayashi fails to disclose the following:

a) a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a part of the insulating layer.

However, Hashimoto et al. ("Hashimoto") discloses a semiconductor region that has the same composition as the low concentration impurity region (For Example: See Paragraph 148). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hashimoto to include a semiconductor region that has the same composition as the low concentration impurity region as disclosed in Hashimoto because it aids in improving resistance (For Example: See Abstract).

Additionally, since Hirabayashi and Hashimoto are both from the same field of endeavor, the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Hirabauashi.

In regards to claim 2, Hirabayashi discloses the following:

a) the pixel TFT has a channel formation region formed above a first wiring line through a first insulating layer and a second insulating layer, and has a low concentration impurity region that is in contact with tile channel formation region and overlaps the first wiring line (For Example: See Figure 3); and

b) the storage capacitor is formed from a capacitor wiring line formed on the same layer as the first wiring line (For Example: See Figure 3).

In regards to claim 2, Hirabayashi fails to disclose the following:

a) a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a part of the insulating layer.

However, Hashimoto discloses a semiconductor region that has the same composition as the low concentration impurity region (For Example: See Paragraph 148). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hashimoto to include a semiconductor region that has the same composition as the low concentration impurity region as disclosed in Hashimoto because it aids in improving resistance (For Example: See Abstract).

Additionally, since Hirabayashi and Hashimoto are both from the same field of endeavor, the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Hirabauashi.

In regards to claim 3, Hirabayashi discloses the following:

a) the pixel TFT has a channel formation region formed above a first wiring line through a first insulating layer, a second insulating layer, and a silicon oxide film, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line (For Example: See Figure 3 and Paragraph 147); and

b) the storage capacitor is formed from a capacitor wiring line formed oil the same layer as the first wiring line (For Example: See Figure 3).

In regards to claim 3, Hirabayashi fails to disclose the following:

a) a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a laminate of the first insulating layer and the silicon oxide film.

However, Hashimoto discloses a semiconductor region that has the same composition as the low concentration impurity region (For Example: See Paragraph 148). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hashimoto to include a semiconductor region that has the same composition as the low concentration impurity region as disclosed in Hashimoto because it aids in improving resistance (For Example: See Abstract).

Additionally, since Hirabayashi and Hashimoto are both from the same field of endeavor, the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Hirabauashi.

In regards to claim 4, Hirabayashi discloses the following:

a) the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (0), titanium (TO, tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films (For Example: See Paragraph 94).

In regards to claim 5, Hirabayashi discloses the following:

a) the channel formation region of the pixel TIFT and the semiconductor region of the storage capacitor are formed of the same semiconductor layer (For Example: See Figure 3).

In regards to claim 6, Hirabayashi discloses the following:

a) the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (TI), barium (Ba), hafrium (Hf), bismuth (Bi), tungsten (W), thorium (Th), and lead (Pb) (For Example: See Paragraph 122).

In regards to claim 9, Hirabayashi discloses the following:

a) the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line (For Example: See Figure 3).

10. Claim 7 is rejected under 35 U.S.C. 103(a) as obvious over Hirabayashi et al. (U.S. Publication No. 2002/0093019) in view of Hashimoto et al. (U.S. Publication No. 2003/0038303) and Someya et al. (U.S. Publication No. 2002/0080295).

In regards to claim 7, Hirabayashi discloses the following:

a) the first wiring line (For Example: See Figure 3)

In regards to claim 7, Hirabayashi fails to disclose the following:

a) floating state.

However, Someya et al. ("Someya") discloses the use of floating state (For Example: See Paragraph 148). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of floating state as disclosed in Someya because it aids in preventing deterioration (For Example: See Paragraph 148 and 149).

Additionally, since Hirabayashi and Someya are both from the same field of endeavor, the purpose disclosed by Someya would have been recognized in the pertinent art of Hirabauashi.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as obvious over Hirabayashi et al. (U.S. Publication No. 2002/0093019) in view of Hashimoto et al. (U.S. Publication No. 2003/0038303) and Murade (U.S. Publication No. 2001/0030722).

In regards to claim 8, Hirabayashi fails to disclose the following:

a) the first wiring line is kept at the lowest power supply electric potential.

However, Murade discloses the use of the lowest potential (For Example: See Paragraph 15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of the lowest potential as disclosed in Murade because it aids in preventing deterioration (For Example: See Paragraph 15).

Additionally, since Hirabayashi and Murade are both from the same field of endeavor, the purpose disclosed by Murade would have been recognized in the pertinent art of Hirabauashi.

12. Claims 11-18 are rejected under 35 U.S.C. 103(a) as obvious over Hirabayashi et al. (U.S. Publication No. 2002/0093019) in view of Seo (U.S. Patent No. 6,323,068), Hashimoto et al. (U.S. Publication No. 2003/0038303) and Murade (U.S. Publication No. 2001/0030722).

In regards to claim 10, Hirabayashi discloses the following:

a) a pixel TFT included in the pixel matrix circuit have a channel formation region formed above a first wiring through an insulating layer, and each have a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line (For Example: See Figure 3); and

b) a storage capacitor included in the pixel matrix circuit is formed from a capacitor wiring line formed on the same layer as the first wiring line (For Example: See Figure 3).

In regards to claim 10, Hirabayashi fails to disclose the following:

a) n-channel TFT included in the driver circuit.

However, Seo discloses the use of a n-channel TFT in the driver circuit (For Example: See Figure 1D and Figure 2A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of a n-channel in the driver circuit as disclosed in Seo because it aids in increasing reliability from disconnection (For Example: See Column 2 Lines 45-67).

Additionally, since Hirabayashi and Seo are both from the same field of endeavor, the purpose disclosed by Seo would have been recognized in the pertinent art of Hirabauashi.

b) a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a part of the insulating layer.

However, Hashimoto discloses a semiconductor region that has the same composition as the low concentration impurity region (For Example: See Paragraph 148). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hashimoto to include a semiconductor region that has the same composition as the low concentration impurity region as disclosed in Hashimoto because it aids in improving resistance (For Example: See Abstract).

Additionally, since Hirabayashi and Hashimoto are both from the same field of endeavor, the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Hirabauashi.

c) the first wiring line connected to the pixel TFT is kept at the lowest power supply electric potential.

However, Murade discloses the use of the lowest potential (For Example: Paragraph 15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of the lowest potential as disclosed in Murade because it aids in preventing deterioration (For Example: See Paragraph 15).

Additionally, since Hirabayashi and Murade are both from the same field of endeavor, the purpose disclosed by Murade would have been recognized in the pertinent art of Hirabauashi.

d) the first wiring line connected to the n-channel TFT is kept at the same level of electric potential as a gate electrode of the n-channel TFT.

However, Seo discloses the use of a n-channel TFT at the same level of potential as a gate electrode (For Example: See Figure 1D and Figure 2C). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of a n-channel TFT at the same level of potential as a gate electrode as disclosed in Seo because it aids in increasing reliability from disconnection (For Example: See Column 2 Lines 45-67).

Additionally, since Hirabayashi and Seo are both from the same field of endeavor, the purpose disclosed by Seo would have been recognized in the pertinent art of Hirabauashi.

In regards to claim 11, Hirabayashi discloses the following:

a) a pixel TFT included in the pixel matrix circuit has a channel formation region formed above a first wiring line through a first insulating layer and a second insulating layer, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line (For Example: See Figure 3); and

b) a storage capacitor included in the pixel matrix circuit is formed from a capacitor wiring line formed on the same layer as the first wiring line (For Example: See Figure 3).

In regards to claim 11, Hirabayashi fails to disclose the following:

a) n-channel TFT included in the driver circuit.

However, Seo discloses the use of a n-channel TFT in the driver circuit (For Example: See Figure 1D and Figure 2A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of a n-channel in the driver circuit as disclosed in Seo because it aids in increasing reliability from disconnection (For Example: See Column 2 Lines 45-67).

Additionally, since Hirabayashi and Seo are both from the same field of endeavor, the purpose disclosed by Seo would have been recognized in the pertinent art of Hirabauashi.

b) a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a part of the insulating layer.

However, Hashimoto discloses a semiconductor region that has the same composition as the low concentration impurity region (For Example: See Paragraph 148). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hashimoto to include a semiconductor region that has the same composition as the low concentration impurity region as disclosed in Hashimoto because it aids in improving resistance (For Example: See Abstract).

Additionally, since Hirabayashi and Hashimoto are both from the same field of endeavor, the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Hirabauashi.

c) the first wiring line connected to the pixel TFT is kept at the lowest power supply electric potential.

However, Murade discloses the use of the lowest potential (For Example: Paragraph 15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of the lowest potential as disclosed in Murade because it aids in preventing deterioration (For Example: See Paragraph 15).

Additionally, since Hirabayashi and Murade are both from the same field of endeavor, the purpose disclosed by Murade would have been recognized in the pertinent art of Hirabauashi.

d) the first wiring line connected to the n-channel TFT is kept at the same level of electric potential as a gate electrode of the n-channel TFT.

However, Seo discloses the use of a n-channel TFT at the same level of potential as a gate electrode (For Example: See Figure 1D and Figure 2C). It would have been obvious to one

having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of a n-channel TFT at the same level of potential as a gate electrode as disclosed in Seo because it aids in increasing reliability from disconnection (For Example: See Column 2 Lines 45-67).

Additionally, since Hirabayashi and Seo are both from the same field of endeavor, the purpose disclosed by Seo would have been recognized in the pertinent art of Hirabauashi.

In regards to claim 12, Hirabayashi discloses the following:

a) a pixel TFT included in the pixel matrix circuit and all n-channel TFT included in the driver circuit each have a channel formation region formed above a first wiring line through a first insulating layer, a second insulating layer, and a silicon oxide film, and each have a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line (For Example: See Figure 3 and Paragraph 148);

b) a storage capacitor included in the pixel in matrix circuit is formed from a capacitor wiring line formed on the same layer as the first wiring line (For Example: See Figure 3).

In regards to claim 12, Hirabayashi fails to disclose the following:

a) n-channel TFT included in the driver circuit.

However, Seo discloses the use of a n-channel TFT in the driver circuit (For Example: See Figure 1D and Figure 2A). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of a n-channel in the driver circuit as disclosed in Seo because it aids in increasing reliability from disconnection (For Example: See Column 2 Lines 45-67).

Additionally, since Hirabayashi and Seo are both from the same field of endeavor, the purpose disclosed by Seo would have been recognized in the pertinent art of Hirabauashi.

b) a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and from a laminate of the first insulating layer and the silicon oxide film.

However, Hashimoto discloses a semiconductor region that has the same composition as the low concentration impurity region (For Example: See Paragraph 148). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hashimoto to include a semiconductor region that has the same composition as the low concentration impurity region as disclosed in Hashimoto because it aids in improving resistance (For Example: See Abstract).

Additionally, since Hirabayashi and Hashimoto are both from the same field of endeavor, the purpose disclosed by Hashimoto would have been recognized in the pertinent art of Hirabauashi.

c) the first wiring line connected to the pixel TFT is kept at the lowest power supply electric potential.

However, Murade discloses the use of the lowest potential (For Example: Paragraph 15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of the lowest potential as disclosed in Murade because it aids in preventing deterioration (For Example: See Paragraph 15).

Additionally, since Hirabayashi and Murade are both from the same field of endeavor, the purpose disclosed by Murade would have been recognized in the pertinent art of Hirabauashi.

d) the first wiring line connected to the n-channel TFT is kept at the same level of electric potential as a gate electrode of the n-channel TFT.

However, Seo discloses the use of a n-channel TFT at the same level of potential as a gate electrode (For Example: See Figure 1D and Figure 2C). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hirabayashi to include the use of a n-channel TFT at the same level of potential as a gate electrode as disclosed in Seo because it aids in increasing reliability from disconnection (For Example: See Column 2 Lines 45-67).

Additionally, since Hirabayashi and Seo are both from the same field of endeavor, the purpose disclosed by Seo would have been recognized in the pertinent art of Hirabauashi.

In regards to claim 13, Hirabayashi discloses the following:

a) the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (0), titanium (TO, tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films (For Example: See Paragraph 94).

In regards to claim 14, Hirabayashi discloses the following:

a) the channel formation region of the pixel TIFT and the semiconductor region of the storage capacitor are formed of the same semiconductor layer (For Example: See Figure 3).

In regards to claim 15, Hirabayashi discloses the following:

a) the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (TI), barium (Ba), hafrium (Hf), bismuth (Bi), tungsten (W), thorium (Th), and lead (Pb) (For Example: See Paragraph 122).

In regards to claim 16, Hirabayashi discloses the following:

a) the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line (For Example: See Figure 3).

In regards to claim 17, Hirabayashi discloses the following:

a) semiconductor device is an active matrix liquid crystal display or an active matrix EL display (For Example: See Paragraphs 2, 4 and 85).

In regards to claim 18, Hirabayashi discloses the following:

a) semiconductor device is a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, or a portable information terminal (For Example: See Figure 16).

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

June 12, 2003

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